CLAIMS

1 . A resistance memory device, comprising:

a memory array comprising a plurality of row lines, a plurality of column lines, and a plurality of resistive elements, each resistive element connected to a row line and a column line, said resistive elements having one of a first resistance value which represents a first logical state and a second resistance value which represents a second logical state;

a sensing circuit for sensing the resistance value of a selected resistance element, said sensing circuit comprising:

a first capacitor and at least one second capacitor;

a charging circuit for charging said capacitors to a predetermined voltage value;

a reference resistance element;

a first discharge circuit for discharging said first capacitor through said selected resistive element and a second discharge circuit for discharging said at least one second capacitors through said reference resistance element; and

a comparison circuit for comparing a discharge characteristic of said first capacitor with a discharge characteristic of said at least one second capacitor.

2. The memory device of claim 1, wherein said at least one second capacitor comprises a first and a second reference capacitor and said associated reference resistance element comprises first and a second resistance elements respectively associated with said first and second reference capacitances having resistance values respectively corresponding to a binary '1' value and a binary '0' value, wherein said first reference capacitor discharges

through said first resistance element, and said second reference capacitor discharges through said second resistance element, the discharging of

3. The memory device as in claim 1 or 2 wherein said comparison circuit compares the voltage levels of said first and at least one second capacitor during the discharging of said capacitors.

4. The memory device of claim 1, further comprising:

a regulation circuit for maintaining a predetermined voltage across said selected resistance element and said reference resistance element during discharge of said capacitors.

5. The memory device of claim 4 wherein said regulation circuit comprises a first regulator associated with said selected resistance element and at least one second regulator associated with said reference resistance

6. The memory device of claim 1, wherein said charging circuit further comprises a switch circuit for selectively connecting said first and at least one second capacitor to a source providing said predetermined voltage value and resistance.

7. The memory device of claim 6 wherein said at least on second capacitor comprises a first reference capacitor and said associated reference resistance element comprises a first reference resistance element, said first reference resistance element having a

resistance value which resides between two possible resistance values for said selected resistance element, said comparison circuit comprising a discharging voltage of said first reference capacitor with a discharge voltage of said first capacitor.

8. The memory device of claim 1 wherein said memory array is an MRAM memory array.

9 . An MRAM memory device, comprising:

a memory array comprising a plurality of row lines, a plurality of column lines, and a plurality of resistive elements, each resistive element connected to a row line and a column line, said resistive elements having one of a first resistance value which represents a first logical state and a second resistance value which represents a second logical state;

a sensing circuit for sensing the resistance value of a selected resistance element, said sensing circuit comprising:

a first capacitor and at least one second capacitor;

a charging circuit for charging said capacitors to a predetermined voltage value;

a reference resistance element;

a first discharge circuit for discharging said first capacitor through said selected resistive element and a second discharge circuit for discharging said at least one second capacitors through said reference resistance element; and

a comparison circuit for comparing a discharge characteristic of said first capacitor with a discharge characteristic of said at least one second capacitor.

10. The MRAM memory device of claim 9, wherein said at least one second capacitor comprises a first and a second reference capacitor and said associated reference resistance element comprises first and a second resistance elements respectively associated with said first and second reference capacitances having resistance values respectively corresponding to a binary '1' value and a binary '0' value, wherein said first reference capacitor discharges through said first resistance element, and said second reference capacitor discharges through said second resistance element, the discharging of

11. The MRAM memory device as in claim 9 or 10 wherein said comparison circuit compares the voltage levels of said first and at least one second capacitor during the discharging of said capacitors.

12. The MRAM memory device of claim 9, further comprising:

a regulation circuit for maintaining a predetermined voltage across said selected resistance element and said reference resistance element during discharge of said capacitors.

13. The MRAM memory device of claim 12 wherein said regulation circuit comprises a first regulator associated with said selected resistance element and at least one second regulator associated with said reference resistance

14. The MRAM memory device of claim 9, wherein said charging circuit further comprises a switch circuit for selectively connecting said first and at least one second capacitor to a source providing said predetermined voltage value and resistance.

15. The MRAM memory device of claim 14 wherein said at least on second capacitor comprises a first reference capacitor and said associated reference resistance element comprises a first reference resistance element, said first reference resistance element having a resistance value which resides between two possible resistance values for said selected resistance element, said comparison circuit comprising a discharging voltage of said first reference capacitor with a discharge voltage of said first capacitor.

16. A method of reading a resistance array, comprising a plurality of column lines, a plurality of row lines, and plurality of resistance elements each connected to a column and row line:

grounding a selected row of said arrays which contain resistance elements to be read;

holding all other rows of said array at a specific voltage;

pre-setting the resistance of a first resistance element connected to said grounded row and associated with a first reference column line to hold a binary '1' resistance value;

pre-setting the resistance of a second resistance element connected to said grounded row and associated with a second reference column line to hold a binary '0' resistance value;

charging a first capacitor associated with a column line of said selected resistance element to a first voltage value;

charging first and second reference capacitors respectively associated with said first and second reference resistance elements to said first voltage value;

discharging said first capacitor through said selected resistance element while discharging said first and second reference capacitors respectively through said first and second resistance elements;

comparing the discharge voltage of said first capacitor with a discharge voltage formed by the discharge rates of said first and second reference capacitors;

determining the binary value held within said selected resistance element as a result of said comparison.

17. A method of reading a resistance array, comprising a plurality of column lines, a plurality of row lines, and plurality of resistance elements each connected to a column and row line:

grounding a selected row of said arrays which contain resistance elements to be read;

holding all other rows of said array at a specific voltage;

pre-setting the resistance of a reference resistance element connected to said grounded row and associated with a first reference column line to reside directly between a binary '1' and a binary '0' resistance value;

charging a first capacitor associated with a column line of said selected resistance element to a first voltage value;

charging a first reference capacitor associated with said reference resistance element to said first voltage value;

discharging said first capacitor through said selected resistance element while discharging said first reference capacitor through said reference resistance element;

comparing the discharge voltage of said first capacitor with a discharge voltage formed by the discharge rates of said first reference capacitor;

determining the binary value held within said selected resistance element as a result of said comparison.

18. The method of claim 16, further comprising:

holding one terminal of said selected resistance element to be read at a constant voltage using the discharge of said first capacitor.

19. The method of claim 16, further comprising:

holding one terminal of first and second reference resistance elements at said constant array voltage using the discharge of said first and second reference capacitors.

20. The method of claim 17, further comprising:

holding one terminal of said selected resistance element to be read at a constant voltage using the discharge of said first capacitor.

21. The method of claim 17, further comprising:

holding one terminal of first and second reference resistance elements at said constant array voltage using the discharge of said first and second reference capacitors.

22. An processor circuit, comprising:

a CPU;

an resistive memory circuit, further comprising:

a memory array comprising a plurality of row lines, a plurality of column lines, and a plurality of resistive elements, each resistive element connected to a row line and a column line, said resistive elements having one of a first resistance value which represents a first logical state and a second resistance value which represents a second logical state;

a sensing circuit for sensing the resistance value of a selected resistance element, said sensing circuit comprising:

a first capacitor and at least one second capacitor;

a charging circuit for charging said capacitors to a predetermined voltage value;

a reference resistance element;

a first discharge circuit for discharging said first capacitor through said selected resistive element and a second discharge circuit for discharging said at least one second capacitors through said reference resistance element; and

a comparison circuit for comparing a discharge characteristic of said first capacitor with a discharge characteristic of said at least one second capacitor.

23. The processor circuit of claim 22, wherein said at least one second capacitor comprises a first and a second reference capacitor and said associated reference resistance element comprises first and a second resistance elements respectively associated with said first and second reference capacitances having resistance values respectively corresponding to a binary '1' value and a binary '0' value, wherein said first reference capacitor discharges through said first resistance element, and said second reference capacitor discharges through said second resistance element, the discharging of

24. The processor circuit as in claims 22 or 23 wherein said comparison circuit compares the voltage levels of said first and at least one second capacitor during the discharging of said capacitors.

25. The processor circuit of claim 22, further comprising:

a regulation circuit for maintaining a predetermined voltage across said selected resistance element and said reference resistance element during discharge of said capacitors.

26. The processor circuit of claim 25 wherein said regulation circuit comprises a first regulator associated with said selected resistance element and at least one second regulator associated with said reference resistance

27. The processor circuit of claim 22, wherein said charging circuit further comprises a switch circuit for selectively connecting said first and at least one second capacitor to a source providing said predetermined voltage value and resistance.

28. The processor circuit of claim 27 wherein said at least on second capacitor comprises a first reference capacitor and said associated reference resistance element comprises a first reference resistance element, said first reference resistance element having a resistance value which resides between two possible resistance values for said selected resistance element, said comparison circuit comprising a discharging voltage of said first reference capacitor with a discharge voltage of said first capacitor.

29. An processor circuit, comprising:

a CPU;

an MRAM memory circuit, further comprising:

a memory array comprising a plurality of row lines, a plurality of column lines, and a plurality of resistive elements, each resistive element connected to a row line and a column line, said resistive elements having one of a first resistance value which represents a first logical state and a second resistance value which represents a second logical state;

a sensing circuit for sensing the resistance value of a selected resistance element, said sensing circuit comprising:

a first capacitor and at least one second capacitor;

a charging circuit for charging said capacitors to a predetermined voltage value;

a reference resistance element;

a first discharge circuit for discharging said first capacitor through said selected resistive element and a second discharge circuit for discharging said at least one second capacitors through said reference resistance element; and

a comparison circuit for comparing a discharge characteristic of said first capacitor with a discharge characteristic of said at least one second capacitor.

30. The processor circuit of claim 29, wherein said at least one second capacitor comprises a first and a second reference capacitor and said associated reference resistance element comprises first and a second resistance elements respectively associated with said first and second reference capacitances having resistance values respectively corresponding to a binary '1' value and a binary '0' value, wherein said first reference capacitor discharges through said first resistance element, and said second reference capacitor discharges through said second resistance element, the discharging of

31. The processor circuit as in claim 29 or 30 wherein said comparison circuit compares the voltage levels of said first and at least one second capacitor during the discharging of said capacitors.

32. The processor circuit of claim 29, further comprising:

a regulation circuit for maintaining a predetermined voltage across said selected resistance element and said reference resistance element during discharge of said capacitors.

33. The processor circuit of claim 32 wherein said regulation circuit comprises a first regulator associated with said selected resistance element and at least one second regulator associated with said reference resistance

34. The processor circuit of claim 29, wherein said charging circuit further comprises a switch circuit for selectively connecting said first and at least one second capacitor to a source providing said predetermined voltage value and resistance.

35. The processor circuit of claim 34 wherein said at least on second capacitor comprises a first reference capacitor and said associated reference resistance element comprises a first reference resistance element, said first reference resistance element having a resistance value which resides between two possible resistance values for said selected resistance element, said comparison circuit comprising a discharging voltage of said first reference capacitor with a discharge voltage of said first capacitor.